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| EXAMINER | |
|---|---|
| AUVE, GLENN ALLEN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 01/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/899,436 | CHUE ET AL. | |
| | Examiner | Art Unit | |
| | Glenn A. Auve | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,14-30,34-40,42 and 43* is/are rejected.

7)☒ Claim(s) *11-13,31-33 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4,5,24,25 and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4 and 24 are rejected because it is not clear what is meant by "predetermined functionalities that remain substantially unchanged over several generations of said electronic architecture." This terminology is very vague and indefinite. What constitutes "substantially unchanged" and "several generations"? The claims do not indicate what the metes and bounds of these limitations are and the specification also appears to be silent with regard to what these terms mean.

Claims 5 and 25 are likewise rejected because it is not clear what is meant by "predetermined functionalities that have a potential to change over several generations of said electronic architecture." This terminology is very vague and indefinite. What constitutes "a potential to change" and "several generations"? The claims do not indicate what the metes and bounds of these limitations are and the specification also appears to be silent with regard to what these terms mean.

Claim 42 is rejected based on lack of positive antecedent basis of "said primary device" and "said auxiliary device".

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3,21-23,42, and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al., U.S. Pat. No. 6,006,319.

As per claim 1, Takahashi et al. (Takahashi) shows a primary device configured to perform core operating functions in the electronic architecture (fig.3,12); an auxiliary device configured to perform selected additional functions in the electronic architecture (14); a primary channel for performing communication procedures between the primary and auxiliary devices (38); and an auxiliary channel configured for performing data transfer between the devices (40), the operations on the primary and auxiliary channels being able to occur in a concurrent manner. Takahashi shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Takahashi also shows that at least on of the primary device and auxiliary device is implemented as an integrated circuit (throughout the specification and inherent in modern computer and electronic systems). Takahashi shows all of the elements recited in claim 2.

As for claim 3, the argument for claim 1 applies. Takahashi also shows that at least on of the primary device and auxiliary device is implemented to include input/output interface functionalities for an electronic system (at least in fig.3, where at least the main or primary unit 12 provides for input/output functionality). Takahashi shows all of the elements recited in claim 3.

As per claim 21, Takahashi shows performing core operating functions of the electronic architecture using a primary device (12 and at least as described in cols. 6-8); performing selected additional functions by using an auxiliary device (14); performing communication procedures between the devices using a primary channel (38); and performing data transfer operations between the devices using an auxiliary channel (40) the operations on the primary and auxiliary channels being able to occur in a concurrent manner. Takahashi shows all of the steps recited in claim 21.

As for claim 22, the argument for claim 21 applies. Takahashi also shows that at least on of the primary device and auxiliary device is implemented as an integrated circuit (throughout the specification and inherent in modern computer and electronic systems). Takahashi shows all of the steps recited in claim 22.

As for claim 23, the argument for claim 21 applies. Takahashi also shows that at least on of the primary device and auxiliary device is implemented to include input/output interface functionalities for an electronic system (at least in fig.3, where at least the main or primary unit 12 provides for input/output functionality). Takahashi shows all of the steps recited in claim 23.

With respect to claim 42 which has been rejected under 35 USC 112, 2nd based on lack of antecedent basis of "said primary device" and "said auxiliary device", the examiner is interpreting the claim as if antecedent basis for the terms had been provided along the same lines as the other independent claims.

As per claim 42, Takahashi shows means for performing core operating functions of the electronic architecture using a primary device (12); means for performing selected additional functions by using an auxiliary device (14); means for performing communication procedures between the devices using a primary channel (38); and means for performing data transfer operations between the devices using an auxiliary channel (40) the operations on the primary

and auxiliary channels being able to occur in a concurrent manner. Takahashi shows all of the steps recited in claim 42.

As per claim 43, Takahashi shows a primary device configured to perform core operating functions in the electronic architecture (fig.3,12); an auxiliary device configured to perform selected additional functions in the electronic architecture (14); a primary channel for performing communication procedures between the primary and auxiliary devices (38); and an auxiliary channel configured for performing data transfer between the devices (40). Takahashi shows all of the elements recited in claim 43.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1,6-10,14-21,26-30, and 34-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Deschepper et al., U.S. Pat. No. 6,145,029 A.

A second prior art rejection is being applied to some of the claims. The claims are so broad that there appear to be many prior art references which anticipate at least the independent claims.

As per claim 1, Deschepper et al. (Deschepper) shows a system for implementing an electronic architecture (fig.1), comprising: a primary device (150) that is configured to perform core operating functions in said electronic architecture; an auxiliary device (100) that is configured to perform selected additional operating functions in said electronic architecture; a

primary channel configured for performing communications procedures between said primary device and said auxiliary device (the control portion of the PCI bus 155); and an auxiliary channel configured for performing data transfer operations between said primary device and said auxiliary device (the data/address transfer portion of the PCI bus 155), said communications procedures over said primary channel and said data transfer operations over said auxiliary channel being able to occur in a concurrent manner. Deschepper shows all of the elements recited in claim 1.

As per claim 21, Deschepper shows performing core operating functions in said electronic architecture by utilizing a primary device; performing selected additional operating functions in said electronic architecture by utilizing an auxiliary device; performing communications procedures between said primary device and said auxiliary device by utilizing a primary channel; and performing data transfer operations between said primary device and said auxiliary device by utilizing an auxiliary channel, said communications procedures over said primary channel and said data transfer operations over said auxiliary channel being able to occur in a concurrent manner (see above regarding the apparatus claim which is implementing the method). Deschepper shows all of the steps recited in claim 21.

Because the apparatus claims and method claims are virtually identical they are being treated together.

As for claims 6 and 26, the argument for claims 1 and 21 apply. Deschepper also shows that said electronic architecture includes a processor (125), said primary device, one or more primary peripheral devices (160,165), a memory (175), said auxiliary device, and one or more auxiliary peripheral devices (at least 185,190,195), wherein said CPU, said memory, and said one or more primary peripheral devices each communicate through said primary device, and

wherein said one or more auxiliary peripheral devices each communicate through said auxiliary device (fig.1). Deschepper shows all of the elements recited in claims 6 and 26.

As for claims 7 and 27, the argument for claims 1 and 21 apply. Deschepper also shows that said primary device includes a CPU interface, one or more peripheral interfaces, a memory interface, a primary channel interface, an auxiliary channel interface, an arbiter, a DMA engine, and an internal primary device bus structure (all inherent in the bridge device structure in that there are interfaces to the processor and memory buses as well as to the peripherals via the PCI bus interface which includes the primary and auxiliary channel interfaces, and the purpose of the bridge is to control transactions among the devices (see col.9) including DMA control (see at least col. 5, lines 40-55)). Deschepper shows all of the elements recited in claims 7 and 27.

As for claims 8 and 28, the argument for claims 1 and 21 apply. Deschepper also shows that an arbiter performs a primary channel arbitration procedure between a processor and one or more primary peripheral devices for controlling access to said primary channel, said primary channel having electrical connectors coupled to pins of said primary device and to pins of said auxiliary device, said electrical connectors being multiplexed to conserve said pins of said primary device and said pins of said auxiliary device (as noted above, arbitration is one of the functions of the bridge device, see col.9, and the connection of the devices via pins is inherent in modern computer systems, and also the PCI bus is a multiplexed bus). Deschepper shows all of the elements recited in claims 8 and 28.

As for claims 9 and 29, the argument for claims 1 and 21 apply. Deschepper also shows that said data transfer operations between said primary device and said auxiliary device over said auxiliary channel are initiated by a processor coupled to said primary device, and then are performed by a direct memory access engine coupled to said primary device (DMA controller

220 in fig.2 controls DMA transfers in the auxiliary device). Deschepper shows all of the elements recited in claims 9 and 29.

As for claims 10 and 30, the argument for claims 1 and 21 apply. Deschepper also shows that said auxiliary device includes a primary channel interface, an auxiliary channel interface, one or more auxiliary configuration registers (216,232), one or more auxiliary peripheral interfaces (212,224,228), and an internal auxiliary device bus structure (all in fig.2, the PCI interface includes the primary and auxiliary channel interfaces). Deschepper shows all of the elements recited in claims 10 and 30.

As for claims 14 and 34, the argument for claims 1 and 21 applies. Deschepper also shows that a processor coupled to said electronic architecture (125) determines whether one of said communications procedures is required between said primary device and said auxiliary device (cols. 5-7). Deschepper shows all of the elements recited in claims 14 and 34.

As for claims 15 and 35, the argument for claims 14 and 34 apply. Deschepper also shows that an arbiter coupled to said primary device performs an arbitration procedure for several entities in said electronic architecture to thereby grant control of said primary channel to said processor (at least in col.9). Deschepper shows all of the elements recited in claims 15 and 35.

As for claims 16 and 36, the argument for claims 14 and 34 apply. Deschepper also shows that said processor communicates with said auxiliary device through said primary device during said one of said communications procedures (at least in cols. 5-7). Deschepper shows all of the elements recited in claims 16 and 36.

As for claims 17 and 37, the argument for claims 1 and 21 apply. Deschepper also shows that a processor coupled to said electronic architecture determines whether one of said data transfer operations is required between a memory device and said auxiliary device, said

processor responsively setting up a direct memory access engine that is coupled to said primary device (cols. 7-8). Deschepper shows all of the elements recited in claims 17 and 37.

As for claims 18 and 38, the argument for claims 17 and 37 applies. Deschepper also shows that said processor instructs said direct memory access engine to initiate said one of said data transfer operations between said memory device and said auxiliary device through said primary device, said direct memory access engine responsively beginning and then controlling said one of said data transfer operations (cols. 7-8 and inherent in what a DMA controller does). Deschepper shows all of the elements recited in claims 18 and 38.

As for claims 19 and 39, the argument for claims 18 and 38 apply. Deschepper also shows that said direct memory access engine determines that said data transfer operation is complete, said direct memory access engine responsively notifying said processor (cols. 7-8 and inherent in the operation of a DMA controller). Deschepper shows all of the elements recited in claims 19 and 39.

As for claims 20 and 40, the argument for claims 1 and 21 apply. Deschepper also shows that an auxiliary direct memory access engine coupled to said auxiliary device determines that one of said data transfer operations is required between a memory device and said auxiliary device, said auxiliary direct memory access engine responsively setting up and controlling said one of said data transfer operations (DMA controller 220, see cols. 7-8). Deschepper shows all of the elements recited in claims 20 and 40.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references also show other systems that include primary and auxiliary devices that are coupled to each other.

8. Claims 11-13,31-33, and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not appear to show the details recited in claims 11,31, and 41.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
January 19, 2004